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CLAIMS

1. A modulator circuit, comprising:

5   a memory for storing interleaved data, the memory having a write address port;

and

an inverse interleaving address generator coupled to the write address port.

2. A modulator circuit as defined in claim 1, wherein the inverse interleaving address

10   generator provides a write address, I, to the memory equal to:

$I = kJ + P$,

where J can be defined as $3*2^n$ or $9*2^n$; $P = A_i/2^m$ and A_i is the requested address; k

$= BROm (A_i \bmod 2^m)$; and $BROm(y)$ = bit-reversed m-LSBs of y.

15   3. A modulator as defined in claim 1, wherein the inverse interleaving address generator

merges the write and read IS-95 interleaving functions as defined in the IS-2000 standard

and combines them into one function.

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4. A modulator as defined in claim 1, wherein the inverse interleaving address generator performs a address mapping function that takes an original row address (A_{OR}) and transfer number (TN) and provides a new row address (A_n) to the memory which follows the equation:

5   If TN = 0 ~ 5, A_n = A_{or}*3;

If TN = 6 ~ 11, A_n = [A_{or}*3] + 1; and

If TN = 12 ~ 17, A_n = [A_{or}*3] + 2.

5. A modulator as defined in claim 1, wherein the modulator comprises a Direct

10   Sequence Spread Spectrum (DSSS) modulator.

6. A modulator as defined in claim 4, wherein the interleaving address generator further comprises:

         a multiply-by-3 circuit;

15   a modulo-6 counter; and

         a modulo 3 counter coupled to the modulo-6 counter and the multiply by 3 circuit.

7. A modulator as defined in claim 1, wherein the inverse interleaving address generator provides addresses to the memory compliant with the IS-95 and the IS-2000 interleaving

20   standards.

8. A modulator as defined in claim 1, wherein the memory includes a read address input

    port, and the modulator further comprises:

    a range selector circuit having an input port for receiving a pseudonoise (PN)

    index or a reverse link frame timing signal and an output port for providing a read

5   address to the memory.

9. A modulator as defined in claim 1, wherein the memory includes a read address input

    port and the modulator further comprises:

    a range selector circuit having an output port for providing a read address to the

10 memory, and the range selector circuit includes a counter and the range selector

    circuit provides a read address [n:0] = counter [(n + 2):2].

10. A modulator as defined in claim 1, wherein the memory includes a data input port and

    the modulator further comprising:

15 a channel encoder having an input port for receiving data; and

    a puncturing circuit having an input port coupled to the channel encoder output port,

    the puncturing circuit having an output port coupled to the data input port of the

    memory.

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11. A modulator as defined in claim 10, wherein the inverse interleaving address generator performs an inverse interleaving function in the case IS-2000 compliant interleaving is required and combines the necessary writing by column and reading by row functions in the case IS-95 compliant interleaving is required.

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12. A Direct Sequence Spread Spectrum (DSSS) modulator, comprising:

a memory for storing interleaved data having a read address port; and

a counter having an output port coupled to the read address port, said counter

5   having a first input port for receiving a pseudonoise (PN) or a reverse link frame

timing signal, and a second input port for receiving a range select signal.

13. A modulator as defined in claim 12, wherein the counter changes state at a rate equal

to modulation data duration for a particular frame of data.

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14. A modulator as defined in claim 12, wherein depending on the Chip Per Modulation

Symbol (CPMS) for a particular frame of data, the addressing of the interleaver

memory is performed by selecting a particular range select signal provided to the

counter.

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15. A method for interleaving data, comprising the steps of:

providing a memory; and

sending a write address, I, to the memory equal to:

$I = kJ + P$,

5   where J can be defined as $3*2^n$ or $9*2^n$; $P = A_i/2^m$ and A_i is the requested address; k

$= BROm (A_i \bmod 2^m)$; and $BROm(y) =$ bit-reversed m-LSBs of y.

16. A method as defined in claim 15, wherein the interleaved data is compliant with the

IS-2000 standard.

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17. A method for interleaving data, comprising the steps of:

    providing a memory; and

    performing an address mapping function that takes an original row address (A_{OR})

and transfer number (TN) and provides a new row address (A_n) to the memory which

5   follows the equation:

    If TN = 0 ~ 5, $A_n = A_{or}*3$;

    If TN = 6 ~ 11, $A_n = [A_{or}*3] + 1$; and

    If TN = 12 ~ 17, $A_n = [A_{or}*3] + 2$.

10   18. A method as defined in claim 17, wherein the interleaved data is compliant with the

IS-95 standard.

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